MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2017/2018

DCS5158 – COMPUTER ARCHITECTURE

(DIT Students Only)

16 OCTOBER 2017
2.30 p.m – 4.30 p.m
(2 Hours)

INSTRUCTIONS TO STUDENT:

1. This question paper consists of 7 pages with **2** sections.
2. Answer **ALL** questions.
3. For **Section A**, shade your answers on the OMR sheet provided.
4. For **Section B**, write your answers in the answer booklet provided.

SECTION A: MULTIPLE CHOICE QUESTIONS (MCQ) (20 Marks)

Instruction: *Answer **ALL** the questions in this section and shade your answers on the OMR sheet provided.*

1. Which of the following is the function of Control Unit?

   A. Coordinates the transfer of data between registers of CPU or microprocessor and ALU.
   B. Provide storage internal to the CPU.
   C. Performs the computer's data processing function.
   D. Provide communication among CPU, memory and I/O.

2. The following are the main structural components of the computer **EXCEPT**:

   A. CPU.
   B. Main Memory.
   C. I/O.
   D. PCI expansion slot.

3. The _____introduced an integrated circuit that enables computer to be faster, cheaper and smaller.

   A. first generation computers
   B. second generation computers
   C. third generation computers
   D. fourth generation computers

4. In a fetch cycle, the _____ interprets instruction and performs the required action.

   A. accumulator
   B. processor
   C. program counter
   D. instruction register

5. Which of the following is the most significant digit of 7452_{10}?

   A. 7
   B. 4
   C. 5
   D. 2

Continued...

6. Convert X = A/B – (C*D+E) * (F/G) to its equivalent Postfix notations.

A. A B / - C D * + E F G * /
B. A B / - C D * E + F G * /
C. A B / C D * E + F G / * -
D. A B / - C D * + E F G / *

7. Opcodes are represented by abbreviations called _____.

A. register
B. mnemonics
C. accumulator
D. stack

8. *"It specifies the operation to be performed. The operation is specified by a binary code"*. This statement refers to _____.

A. source operand reference
B. operation code
C. result operand code
D. next instruction reference

9. Principal advantage for this addressing mode is no memory reference. Which of the following addressing modes that refer to the statement?

I. Direct addressing.
II. Immediate addressing.
III. Register addressing.
IV. Stack addressing.

A. I and II
B. I, II and III
C. III and IV
D. II, III and IV

10. Which of the following types of instruction provides computational capabilities for processing numeric data?

A. Arithmetic instruction.
B. Branch instruction.
C. I/O instruction.
D. Test instruction.

Continued...

11.

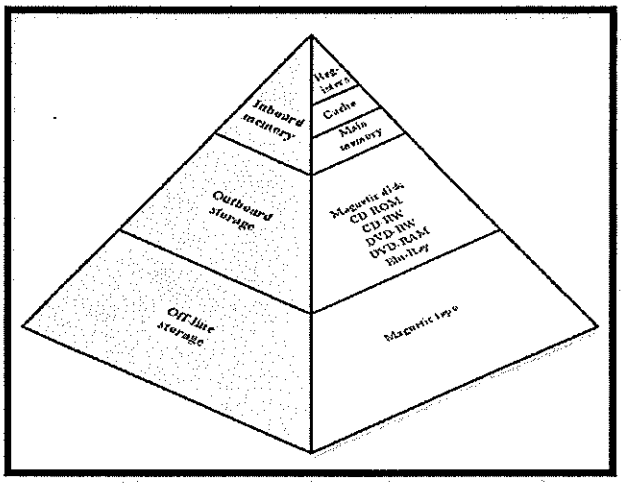

Figure 1: The memory Hierarchy

A typical hierarchy is illustrated in Figure 1. As one goes down the hierarchy, which of the following does **NOT** occur:

A. Decreasing cost per bit.
B. Increasing capacity.
C. Reducing access time.
D. Decreasing frequency of access of the memory by the processor.

12. All of the following are non-volatile **EXCEPT**:

A. ROM
B. EPROM
C. DROM
D. RAM

13. The data lines provide a path for moving data among system modules. These lines, collectively, are called _____.

A. data Bus
B. data Collection
C. control Bus
D. address Bus

Continued...

14. To extend the connectivity of the processor bus, we use _____.

A. PCI bus
B. SCSI bus
C. Controllers
D. Multiple bus

15. The main advantage of multiple bus organization over single bus is _____.

A. reduction in the number of cycles for execution
B. increase in size of the registers
C. better Connectivity
D. none of these

16. Video cards are connected to the memory, chipset and processor via the _____.

A. Universal I/O bus
B. Peripheral I/O bus
C. Serial I/O bus
D. Local I/O bus

17. The method of synchronizing the processor with the I/O device in which the device sends a signal when it is ready is known as _____.

A. Exceptions
B. Signal handling
C. Interrupts
D. DMA

18. Which of the following are categories of external devices?

I. Human readable
II. Machine readable
III. Communication
IV. Memory

A. I, II and III
B. I, II and IV
C. II and IV
D. I, II and IV

Continued...

19. Four general categories of techniques that are in common use in I/O device are _____

A. Multiple interrupt lines, Software poll, Daisy chain (hardware poll, vectored) and Bus arbitration (vectored).
B. Control logic, Rose Chain, International Reference Alphabet (IRA), Data buffering.
C. Bus arbitration (vectored), Rose Chain, direct memory access (DMA), Data buffering.
D. Control logic, Rose Chain, Multiple interrupt lines, direct memory access (DMA).

20. _____ is a key implementation technique used to build fast processors that can be seen in RISC architecture.

A. Querying
B. Pipelining
C. I/O Module
D. Interrupt Driven I/O

Continued...

SECTION B: STRUCTURED QUESTIONS (80 Marks)

Instruction: *Answer ALL the questions in this section and write your answers in the answer booklet provided.*

QUESTION 1

a) List and briefly explain any **FOUR** registers with its function. (8 marks)

b) Perform the following conversion. All the necessary steps to obtain the answer must be shown.

i. Convert 11101.01_2 to its decimal equivalent. (2 marks)
ii. Convert $4F.7A_{16}$ to its binary equivalent. (2 marks)
iii. Convert 571_8 to its hexadecimal equivalent (3 marks)

c) Calculate $40_{10} - 72_{10}$ by using two's complement with 8-bit binary representation. (5 marks)

[TOTAL: 20 MARKS]

QUESTION 2

a) Given the following expression:

$$Z = ((F / G) + (H * J)) / (I - K / L)$$

i. Convert the expression to postfix notation. (2 marks)
ii. Based on the expression in the above question, write the following machine instructions:
- Zero-address (2 marks)
- One-address (2 marks)
- Two-address (2 marks)

b) A computer system has a memory architecture made up of main memory of 1GB and cache of 512 KB. In order to perform an efficient mapping function, the main memory is arranged in block of 32 bytes.

Draw the address structures for different mapping functions as below. Indicate the fields and the number of bits required for each field

i. Direct Mapping (4 marks)
ii. Two Way Set Associative Mapping (4 marks)

c) List and explain any **TWO** parameters to measure the performance of memory. (4 marks)

[TOTAL: 20 MARKS]

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QUESTION 3

a) What is the difference between the local I/O bus and standard I/O bus? Give one example for each. (6 marks)

b) Briefly explain **TWO** types of system bus as given below:
   i. Address buses (2 marks)
   ii. Data buses (2 marks)

c) Define Peripheral Component Interconnect Express(PCIe). State **TWO** key requirements for PCIe. (4 marks)

d) I/O modules must communicate with the processor and the external devices. This is called as processor communication. List and explain any **THREE** activities involved in this communication process. (6 marks)

[TOTAL: 20 MARKS]

QUESTION 4

a) Calculate the ***Throughput*** and ***Speedup*** for the implementation of non-pipelining and pipelining with **SIX** instructions where each instruction has 4 stages (FI, DI, EI, WO) with delay of 3, 3, 4 & 3 respectively. (10 marks)

b) Explain **THREE** possible techniques for I/O operations. (6 Marks)

c) To execute an I/O-related instruction, the processor issues an address, specifying the particular I/O module and external device, and an I/O command. There are four types of I/O commands that an I/O module may receive when it is addressed by a processor. List **FOUR** types of I/O commands. (4 Marks)

[TOTAL: 20 MARKS]

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